P1P3800A

Phase Synchronizing Clock Generator

ON Semiconductor®

http://onsemi.com

Product Description

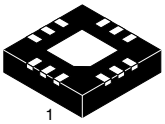
P1P3800A is a Phase Synchronizing clock generator that generates four outputs from an input clock. Output frequency will be a divide by two of the input clock. The phase of the output clocks is selectable through four select signals S1, S2, S3 and S4. Refer to *Output Clock Selection Table*. The outputs will go 'low' when all the select signals are 'low'. The transition to a new state of the output will be 'glitch free' when the select inputs change state. A Power Down signal enables the device to be driven to a power save mode, when active. The device works over a supply voltage range of 3.8 V – 5.5 V. The device is available in a 12–Lead 3mmx3mm WQFN package and operates over -40°C to +85°C.

Features

- Input Clock Frequency:
  120 Hz – 240 Hz (External Reference Clock)
- Output Clock Frequency:
  60 Hz – 120 Hz
- 4 Clock Outputs
- 4 Two Level Controls to Select Sets of Clock Outputs
- Output Buffer Drive Strength: 8 mA
- Supply Voltage: 3.8 V – 5.5 V
- Power Down for Power Save
- 12–Lead 3mmx3mm WQFN Package
- Operating Temperature Range: -40°C to +85°C
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Application

- P1P3800A can be used in applications where Phase Synchronization is needed.

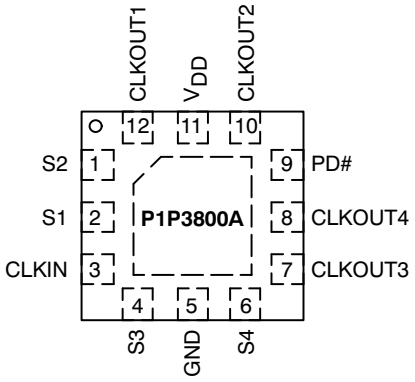


WQFN12
CASE 510AH

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION



(Top–View)

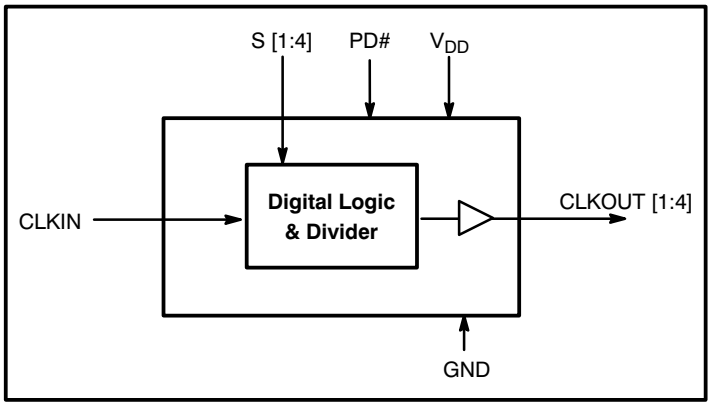


Figure 1. Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

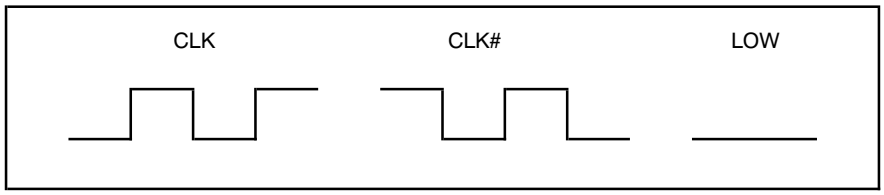
Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	S2	I	Output clock select. Refer *Output Clock selection* table. Has NO default state
2	S1	I	Output clock select. Refer *Output Clock selection* table. Has NO default state.
3	CLKIN	I	External Reference Clock Input
4	S3	I	Output clock select. Refer *Output Clock selection* table. Has NO default state.
5	GND	P	Ground to entire chip
6	S4	I	Output clock select. Refer *Output Clock selection* table. Has NO default state.
7	CLKOUT3	O	Buffered clock output. Refer *CLKOUT Diagram*
8	CLKOUT4	O	Buffered clock output. Refer *CLKOUT Diagram*
9	PD#	I	Power Down. Powers down the entire chip when pulled LOW. CLKOUT [1:4] will be LOW when power down is enabled. Has NO default state.
10	CLKOUT2	O	Buffered clock output. Refer *CLKOUT Diagram*
11	V_{DD}	P	Supply Voltage
12	CLKOUT1	O	Buffered clock output. Refer *CLKOUT Diagram*

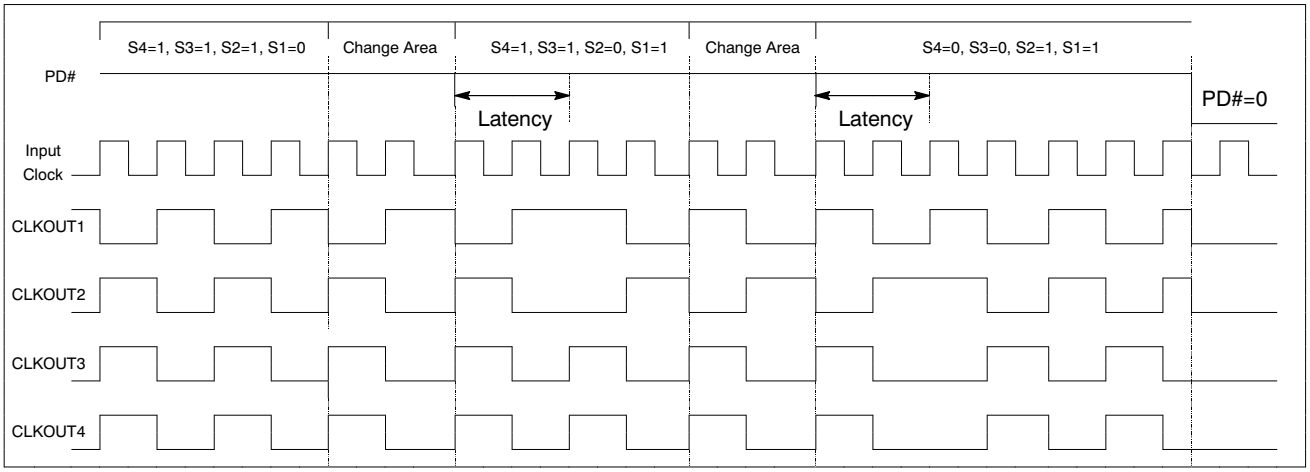
Table 2. OUTPUT CLOCK SELECTION TABLE

S4	S3	S2	S1	CLKOUT4	CLKOUT3	CLKOUT2	CLKOUT1
0	0	0	0	Low	Low	Low	Low
0	0	0	1	CLK#	CLK#	CLK#	CLK
0	0	1	0	CLK#	CLK#	CLK	CLK#
0	0	1	1	CLK#	CLK#	CLK	CLK
0	1	0	0	CLK#	CLK	CLK#	CLK#
0	1	0	1	CLK#	CLK	CLK#	CLK
0	1	1	0	CLK#	CLK	CLK	CLK#
0	1	1	1	CLK#	CLK	CLK	CLK
1	0	0	0	CLK	CLK#	CLK#	CLK#
1	0	0	1	CLK	CLK#	CLK#	CLK
1	0	1	0	CLK	CLK#	CLK	CLK#
1	0	1	1	CLK	CLK#	CLK	CLK
1	1	0	0	CLK	CLK	CLK#	CLK#
1	1	0	1	CLK	CLK	CLK#	CLK
1	1	1	0	CLK	CLK	CLK	CLK#
1	1	1	1	CLK	CLK	CLK	CLK

CLKOUT Diagram

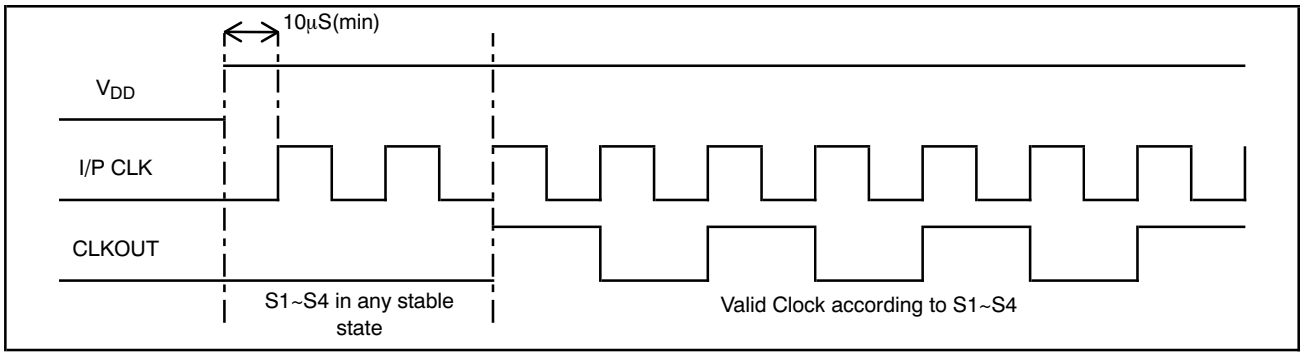


TIMING Diagram For Glitch Free Operation (For Reference)
(Transition of outputs from any state to any other state)



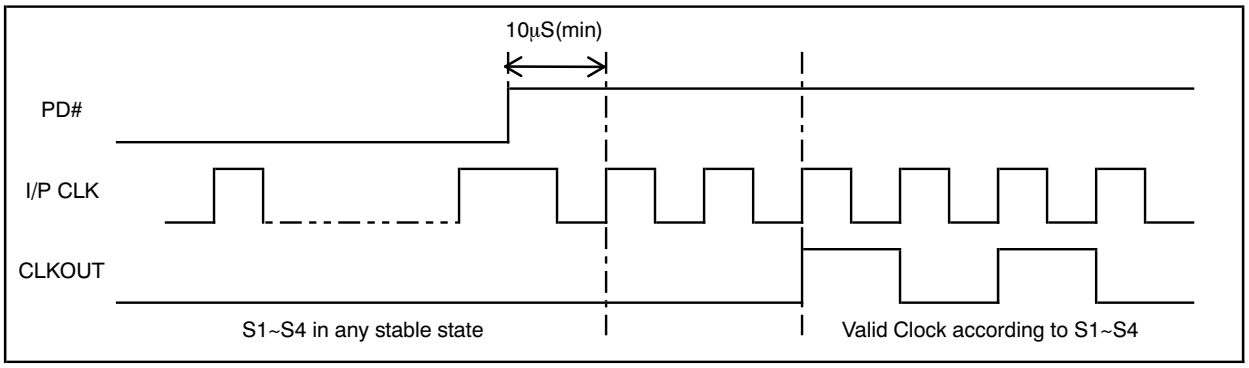
Note: Transition to new state will happen after a latency of one output clock cycle after completing the present output clock cycle
Transition to new state will happen after a latency of up to 3 input clock cycles excluding the input cycle where the transition has occured.

Power Up



Note: Transition to new state will happen after a latency of up to 2 input clock cycles excluding the input cycle where the transition has occured.

PD# Operation



Note: Transition to new state will happen after a latency of up to 2 input clock cycles excluding the input cycle where the transition has occured.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	3.8	5.5	V
T_A	Operating Temperature	−40	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7.0	pF

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	Voltage on V_{DD} pin with respect to Ground	−0.5 to +7.0	V
V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +4.0	V
T_{STG}	Storage Temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22−A114−B)	2.0	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Operating Voltage		3.8	5.0	5.5	V
V_{IL}	Input Low Voltage (Note 1)		GND − 0.3		0.8	V
V_{IH}	Input High Voltage (Note 1)		1.6		3.0	V
I_{IL}	Input Low Current				10	μA
I_{IH}	Input High Current				10	μA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −8 mA	V_{DD} − 0.6*			V
I_{CC}	Power Down Current (PD# pulled to GND)			1.0		μA
I_{DD}	**Dynamic Supply Current, PD# = 5.5 V; S[1:4] = 5.5 V/GND; CLKIN Swing = 0 to 5.5 V; V_{DD} = 5.5 V				1.8	mA
	Dynamic Supply Current, PD# = 3 V; S[1:4] = 3 V/GND; CLKIN Swing = 0 to 3.0 V				3.0	
	Dynamic Supply Current, PD# = 3 V; S[1:4] = 1.6 V; CLKIN Swing = 0 to 1.6 V				4.0	
	Dynamic Supply Current, PD# = S[1:4] = 1.6 V; CLKIN Swing = 0 to 1.6 V				5.0	

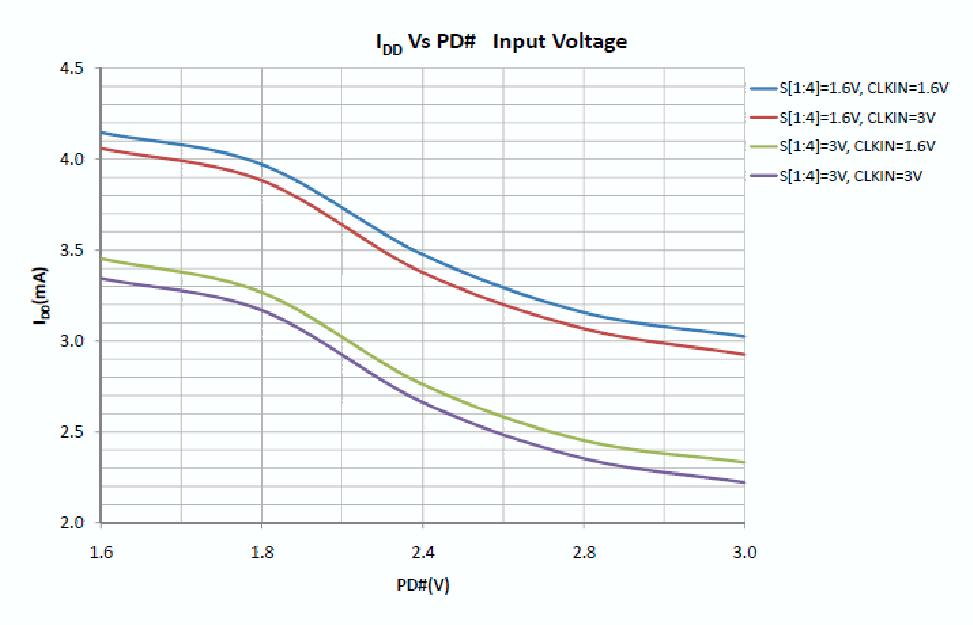
*For V_{DD} = 5 V, V_{OH} = V_{DD} − 0.4 V.
**Indicative value, not a recommended operating condition.
1. Parameter is guaranteed by design and characterization. Not tested in production.

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
CLKIN	Input Clock Frequency	120		240	Hz
CLKOUT	Output Clock Frequency	60		120	Hz
t_{LH}, t_{HL}	Output Rise / Fall time (Measured from 20% to 80%) (Notes 1, 2)			10	µs
t_{LH}, t_{HL}	Input Rise / Fall time (Measured from 20% to 80%)			50	µs
t_{DOUT}	Output Duty Cycle (Measured at V_{DD}/2) (Notes 1, 2)	49	50	51	%
t_{DIN}	Input Duty Cycle	49	50	51	%
t_{su}	Set up time for control signals, S[1:4], PD# to input clock rising edge (Note 1)	60			µs
t_h	Hold up time for control signals, S[1:4], PD# to input clock rising edge (Note 1)	60			µs
t_{skew}	Output−Output Clock Skew (Note 1)			10	µs

2. All parameters are specified with 15 pF loaded output.

Typical I_{DD} Vs PD# Input Voltage Plot



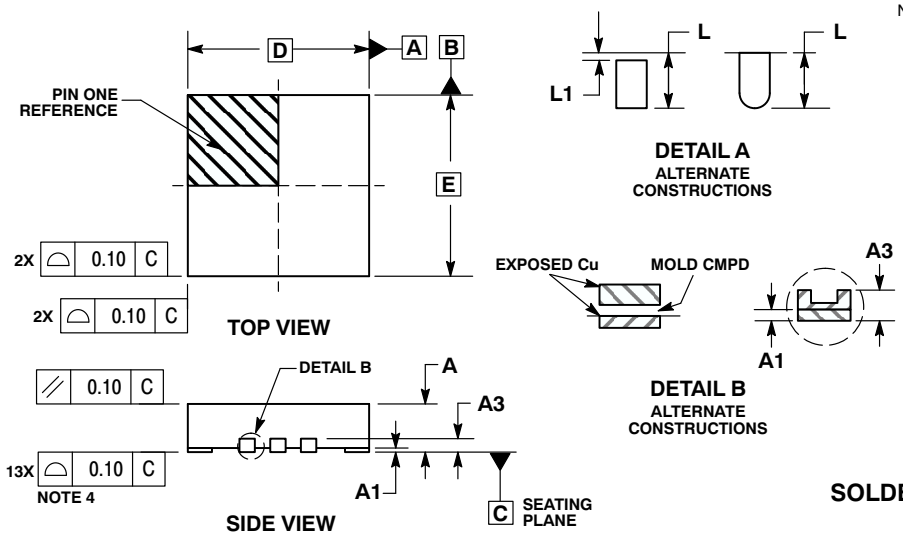
ORDERING INFORMATION

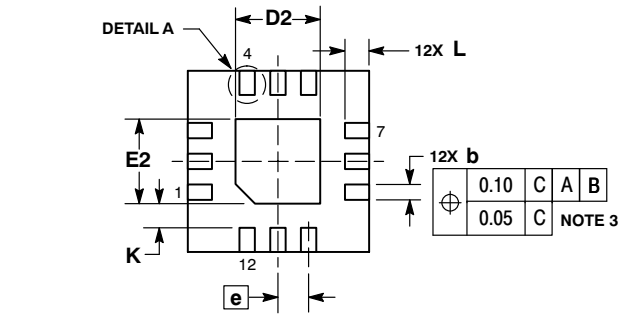
Part Number	Package	Shipping†
P1P3800AG12CRTWG	12 pin (3 mm x 3 mm) WQFN	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WQFN12 3x3, 0.5P
CASE 510AH
ISSUE O

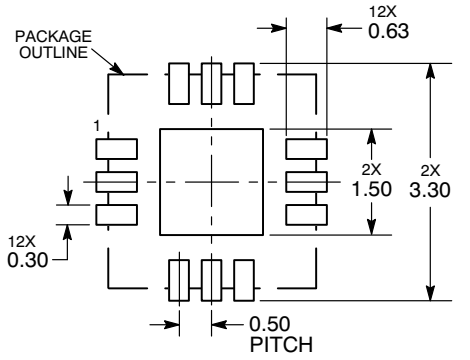




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.65	0.85
A1	0.00	0.05
A3	0.22 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.30	1.50
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

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